Electrocardiography (EKG) System

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CONTENTS

I. Background

This paper will outline the design and testing process to develop a simple EKG to measure a person's heart-rate. The components of the EKG include the I-amp and integrator, the anti-aliasing filter, the isolator, the power supply, and the input RC network.

The I-amp needed to let very low frequency signals through but block DC voltages. To accomplish this, a passive RC filter was added at each input with a break point frequency of 0.05 Hz. The frequencies of the heart-rate above 500 Hz need to be attenuated by 72 dB to prevent the ADC in the AD2 from aliasing. The isolator section uses an optocoupler to separate the signal coming out of the anti-aliasing filter to the AD2. This is required as the original signal and power supply contain noise. The electrical signal coming off the subject's body is very low in amplitude (roughly 500 uV). This is why the I-amp section was designed to have a gain of around 1000. Further requirements are described in the calculations section.

II. Schematics and Calculations of Subsystems

A. Power Supply

The purpose of the power supply is to provide 3.3V to active components in the EKG System. We need two separate power lines to power both sides of the Isolator, which handles interference. The power supply uses an LT1121CN8 to step the 9 volts from the battery down to 3.3 volts to be used by the circuit components on the input side of the isolator. The power supply can be seen in Fig. 1. The purpose of capacitors C_1 and C_2 is to filter out any high frequency noise from the input and the output of the regulator. These were both set to $0.1\mu F$. The purpose of the the J5 jumper is to allow the user to power the isolated section from the AD2 power supply as well. This will be used when testing the circuit.

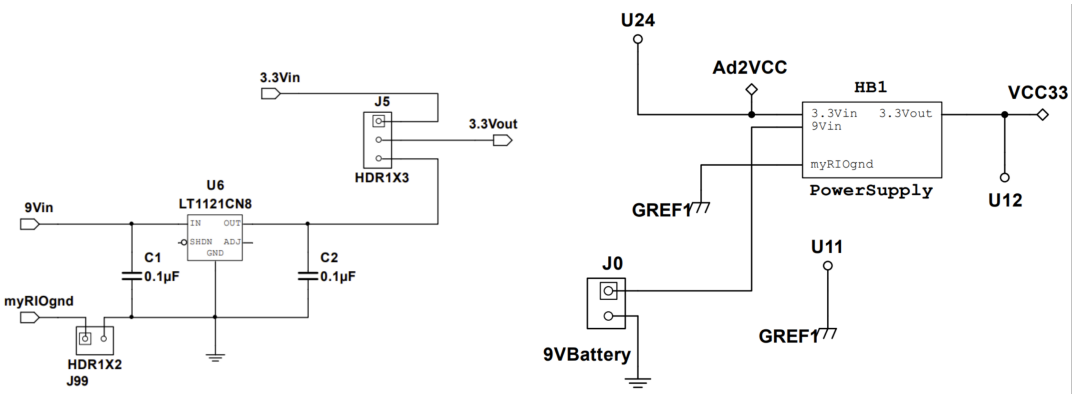

Fig. 1. Internal Power Supply Schematic and Top Level Power Supply System

B. Isolator

The purpose of the isolator is to isolate the signal coming from the filter to the AD2 and isolate the power supplies of both of them. The isolator chosen was the IL300. The isolator is configured in a unipolar isolation amplifier. The equations needed to desing this kind of isolator were found in [1] and can be seen below:

$$G = k_3 * \frac{R_2}{R_1}$$

$$R_1 = \frac{V_{inmax}}{K_1 * I_{omax}}$$

$$R_2 = \frac{R_1 * G}{K_3}$$

The V_{inmax} term is the maximum expected input voltage to the isolator. Given the fact that the supply voltage is 3.3 volts, this value was also set to 3.3 volts. The I_{omax} term is the maximum current that is allowed to flow through the transmitting LED. The average value of this was found to be 10 mA from [2] and this was set to that value. The K values are the gains of the different transmitting and receiving LEDs in the optocoupler. These values were given in [1]. The K_1 value is typically 0.012 and the K_3 value is typically 1.377. The gain (G) was set to 1. With these values, R_1 was calculate to be 27500Ω. A $27k\Omega$ was chosen as its value. R_2 was calculated to be 19607.84Ω. An 18Ω resistor was chosen. This resistor was also the "Do not install" value that our group decided on. These resistors are R_12 and R_14 respectively. The resistor the is in series with the transmitting resistor was chosen to be 120Ω to limit the current through the LED in a fault condition of the op amp.

The schematic of the isolator section is seen in Fig. 2. The extra unity gain op amps that have nothing connected to the either outputs are a result of there being two op amps in the LMC6482AIN package. The op amps on the input and output of the isolator cannot be from the same IC because they need to be isolated. Connected in the extra op amps like this keeps them from floating and potentially creating interference. The expected gain of the isolator from the chosen R_2 is 0.918.

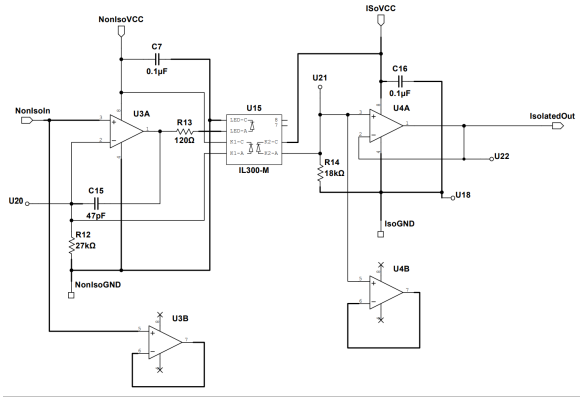

Fig. 2. Schematic of the Isolator Section

C. Butterworth Filter

The requirements for the butterworth filter were a 72 dB attenuation at 500 Hz and a 4th order design. The 4th order design was accomplished by cascading two 2nd order Sallen-Key filters together where the system with the lowest Q value was first. Both of these Sallen-Key filters are housed in the same op amp IC. This IC has a capacitor across its supply lines (C_{14}). This was chosen to be $0.1\mu F$, the same as the ones used in the power supply. Because the system is 4th order low pass, the magnitude of the response drops 80 dB per decade after the break point frequency. The break point of the filter was found to make a 72 dB attenuation at 500 Hz.

$$f_c = \frac{500Hz}{10^{\frac{72dB}{80dB}}} = 62.95Hz$$

To find the capacitor and resistor values for the two 2nd order filters, a program was written in python. This program can be seen in the Appendix in Fig. 28. This program, accepts the break point frequency and Q value as inputs and outputs $R_1, R_2, C_1, and\ C_2$ corresponding to the generic schematic in Fig. 3.

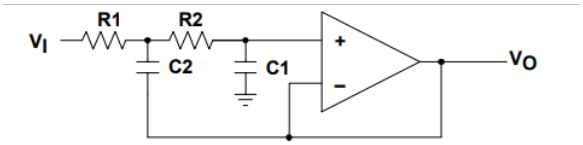

Fig. 3. Generic Sallen-Key Filter Schematic with Unity Gain

The equations used in the program are simplifications of the main Sallen-Key low pass equations and can be found in [3]. They can be seen below:

$$R_1 = mR, R_2 = R, C_1 = C, C_2 = nC$$

$$f_c = \frac{1}{2\pi RC\sqrt{mn}}, Q = \frac{\sqrt{mn}}{m+1}$$

Taken from a Butterworth filter table, cascading two 2nd order filters together to create a 4th order Butterworth response requires a filter with a Q value of 0.5412 first and another 2nd order filter with a Q value of 1.3065 second. These values were entered into the program and the following values were found for the first filter: $R_1 = 220k\Omega$, $R_2 = 270k\Omega$, $C_1 = 0.01uF$, and $C_2 = 0.01uF$. The Q value for this filter was 0.497 and the break point frequency was 65.29 Hz. The following values were found for the second filter: $R_1 = 47k\Omega$, $R_2 = 150k\Omega$, $C_1 = 0.01uF$, and $C_2 = 0.1uF$. The minimum resistor value is $47k\Omega$. The Q value for this filter was 1.347 and the break point frequency was 59.97 Hz. The break points deviate slightly on

either side of the calculated break point, this will be fine as the overall break point will resemble the average of the two. The Q values also deviate from the ideal ones but this will be fine. The final schematic of the filter can be seen in Fig. 4.

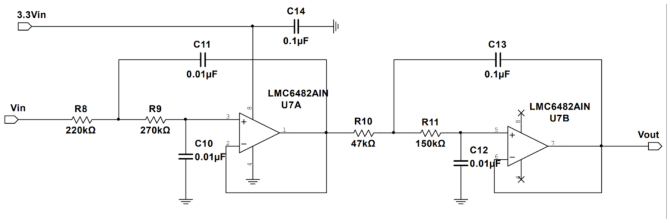

Fig. 4. Butterworth Internal Schematic

D. Integrator Offset (Vmid)

The circuit used to generate a constant value for V_{mid} can be seen in Fig. 5. This value is used an input to the integrator to keep the output of the I-amp at a constant DC bias. Because the power supply is single poled, this value should be half of the supply voltage. In the case of 3.3 volts, this should be 1.65 volts. This is accomplished with a voltage divider and low pass filter fed through an op amp buffer. It should be mentioned that the op amp has a capacitor across the power supply lines (C_9) this set to $0.1uf$, the same as the other ones. The requirement of V_{mid} to be half of the supply implies that the resistor values should be the same. The design requirements state that the Thevenin input resistance of the network should be between $25k\Omega and 100k\Omega$. Because it is a voltage divider, the Thevenin equivalent input resistance is the parallel combination of the resistors. For resistors of equal value, this is half of one of their values. We chose $100k\Omega$ as the value for R_6 and R_7. This makes the equivalent input resistance $50k\Omega$. The design requirements also state that the break point of the network should be in between 2 Hz and 5 Hz. The network is a first order system with C_8 as the capacitor and the equivalent resistance as the resistor. The equation for the break point can be seen below:

$$f_c = \frac{1}{2\pi R_{eq} C}$$

Using a capacitor value of $1uf$ the break point becomes 3.18 Hz which is within the design requirements.

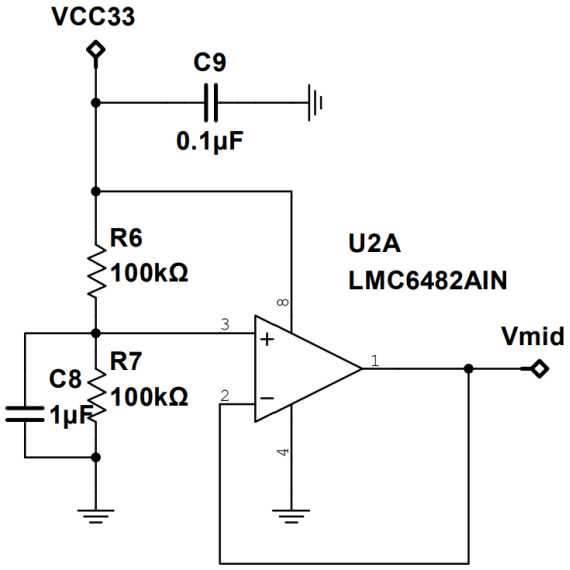

Fig. 5. Schematic of Vmid Reference Generator

E. RC Filters

The requirements for the two RC networks feeding into the I-amp were to have resistors between $250k\Omega \; and \; 300k\Omega$. The break point of the first-order RC filters also had to be between $0.05Hz \; and \; 0.1Hz$. We chose the same break point for both input jacks as shown in Fig. 6. The resistance component is within the required range and the break frequency is as follows.

$$f_c = \frac{1}{2\pi RC} = 0.0589Hz$$

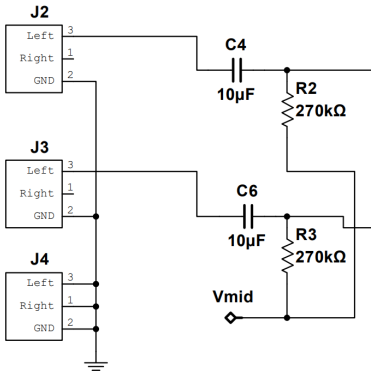

Fig. 6. RC Network Schematic and Parts

F. Instrumentation Amplifier

The instrumentation amplifier consists of the I-amp IC and an integrator using an LMC6482AIN. Following the input RC networks, the two inputs go to the inverting and Non-inverting inputs of an AD623 instrumentation amplifier. This amplifier amplifies the difference between the two inputs. The gain resistor chosen was initially 56Ω. This value was later changed during testing as the data-sheet (seen here [4]) specifies that the minimum gain resistor value is 100Ω. The relationship between the gain resistor and the gain is seen in the equation below:

$$R_G = \frac{100k\Omega}{G-1}$$

With $R_G = 56\Omega$, the gain would be 1818.2. In hindsight, this gain is a lot higher than it needs to be, and according to the datasheet table, the lowest gain resistor used is 100Ω, which is why we changed this value during testing. 100Ω has a gain of 1000.

When the I-amp is being used with a very large gain, dc offset of the output tends to drift and is not guaranteed to be 0 volts. This problem can be solved by passing the output through an integrator and back into the feedback pin of the AD623. The schematic can be seen in Fig. 7.

G. Integrator

The project requirement specifies that the integrator needs to have a transfer function of between:

$$H(s) = \frac{-1}{s}, H(s) = \frac{-1}{10s}$$

Given that the generic transfer function of an integrator is:

$$H(s) = \frac{-1}{sRC}$$

The value of the RC must be between 1 and 10. Choosing a value of $1M\Omega$ for the resistor (R_4) and a value of $1uf$ for the capacitor (C_3) gives an RC value of 1 which is in the specified range. Inputting a voltage into the non-inverting input of the op amp used with the integrator makes it center the output voltage at that value. V_{mid} is input here to center the output of the I-amp section at 1.65 volts. The schematic can be seen in Fig. 7.

III. Multisim Simulations of Subsystems

The simulations of the expected signals are shown for the each subsystem below.

A. Power Supply

To validate the power supply, we ran a transient at the 9V input and VCC33 output as shown in Fig. 8. This produced a DC signal of 3.3V at VCC33 as expected. We chose to test these points because it validates the power supply, but also corresponds to the test points U12 and AD2VCC, which will make testing easier.

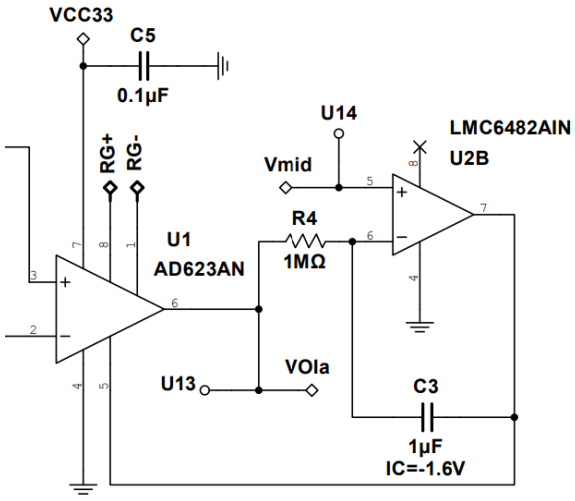

Fig. 7. I-Amp Subsection Schematic

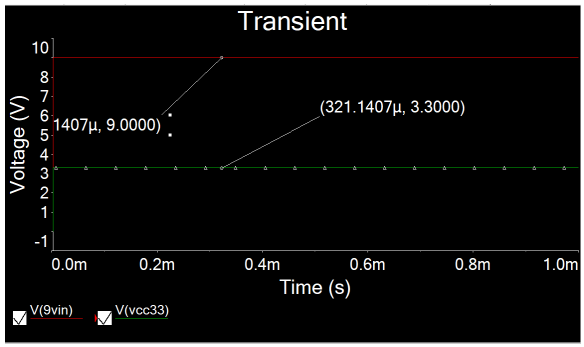

Fig. 8. Power Supply Transient Test

B. Isolator

The isolator was tested in Multisim by inputting a 30 Hz sine wave with an amplitude of 750 mV and an offset of 1.65 (this matches what the filter will output). The output and input are shown in a Multisim transient analysis in Fig. 9. The amplitudes of the input and output are indicated in the figure.

Subtracting 1.65 volts from the peak voltage of the output gives a peak voltage of 550.9 mV. Considering the input is 750 mV, this gives a gain of 0.735. While this is not the 0.918 gain that was calculated, this can be attributed to how Multisim handles the K values of the optocoupler.

C. Butterworth Filter

The Butterworth filter was tested in Multisim but running an AC Sweep through the filter to confirm the correct break point and pass-band gain of 1. The input signal had an amplitude of 1 volt and a DC offset of 1.65 volts. This test can be seen in Fig. 11.

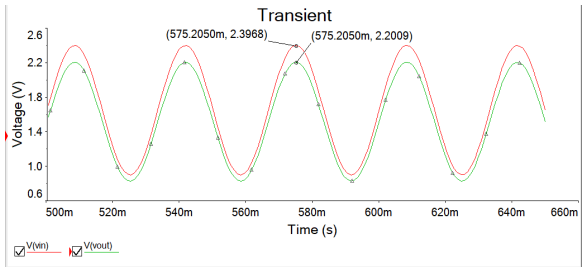

Fig. 9. Transient of Isolator Multisim Test

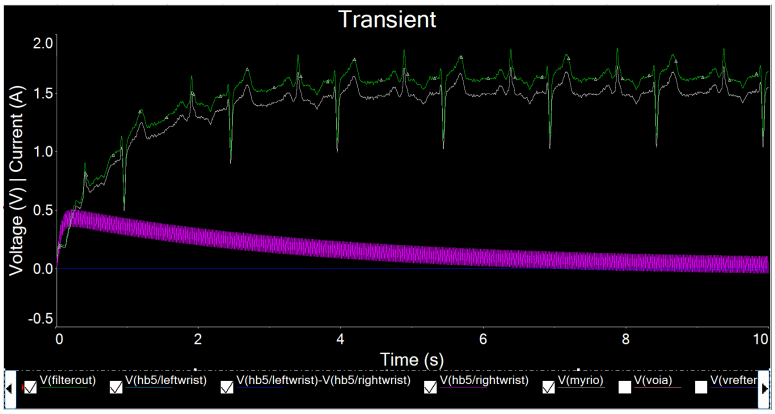

Fig. 10. Isolator Output with EKG Signal (grey)

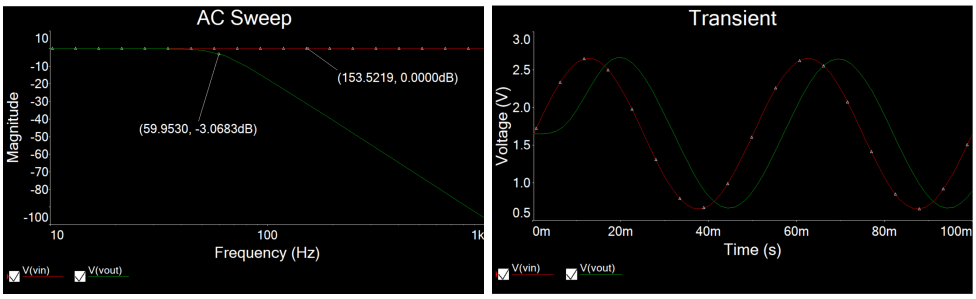

Fig. 11.
AC Sweep Test: Input: 10Hz to 1kHz, Expecting break frequency at -3.01 dB
Transient Test: Input: 20Hz, 1Vpk with 1.65 V Offset, Frequency below the corner frequency

To test the Butterworth filter, we will remove all ICs except for U7 as this is the one that contains the op amp used in the Butterworth filter. The two grounds will be connected with J99 and a jumper will be used to allow the AD2 to power both sections of the circuit. The positive power supply of the AD2 will be set to 3.3 volts and connected to U24 and the ground of the AD2 will be connected to U10. The wavegen of the AD2 will be connected to test point U13 and the first scope input and the second scope input will be connected to U16. An AC sweep will be run with the AD2 from 20 Hz to 500 Hz with a sine wave of amplitude of 1 volt and a DC offset of 1.65 volts. The -3 dB point will be measured as well as the -72 dB point.

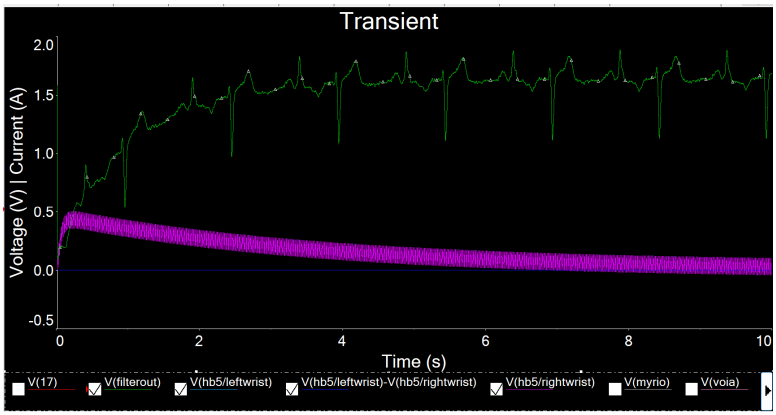

Fig. 12. Filter Output with EKG Signal (green)

D. Integrator Offset (Vmid)

The vmid section was built in Multisim and a transient was taken of the output voltage. The VCC supply in Multisim was set to 3.3 volts with a 1kHz sine wave of 0.1 volt amplitude riding on it to simulate power supply interference. The output voltage stayed at a constant 1.65 volts. This test can be seen in Fig. 13.

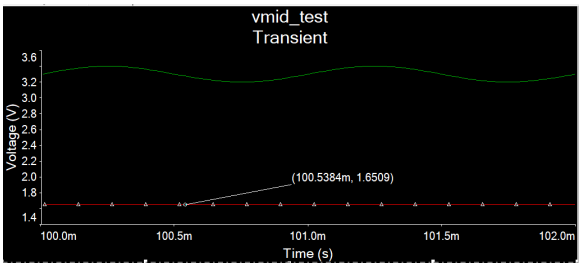

Fig. 13. Transient of Vmid Multisim Test

The test plan for this part consists of removing all ICs except for U2 and grounding the output of the I-amp. This is because the integrator is also part of U2 and the input would be floating if the output of the i-amp was not grounded. The two grounds are connected with J99 and the jumper is installed to enable the AD2 to power the entire board. The positive power supply of the AD2 will be set to 3.3 volts and connected to U24 and the ground of the AD2 will be connected to U10. The voltage on the output of the V_{mid} generator will be measured and ideally will show a 1.65 volt DC signal as seen in the Multisim test.

E. RC Filters

To validate our calculations and that our break frequency is meets our requirements we ran an AC Sweep on both of the RC filters (which have the same component values). As shown in Fig. 14, the break frequency is $\approx 0.0597Hz$, which is within the bounds of $0.05Hz$ *and* $0.1Hz$.

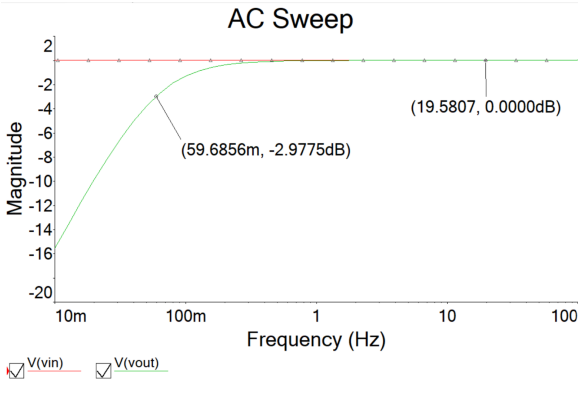

Fig. 14. AC Sweep: 1Vpk 0.01Hz to 100Hz

F. Instrumentation Amplifier with Integrator

To validate the instrumentation amplifier we ran a transient with the input jack signals as shown to produce the output at the VOIa test point in Fig. 15. With our gain resistor 100 to get a gain of 1000 for testing, this is about what we expected. We want VOIa to be the result of amplifying the the differences in the input signal. It can be seen that it amplifies the difference between the two input signals roughly 1000 times.

Fig. 16 shows the output of the Inamp with the EKG signal as an input. It takes in the left and right signals given from the isolator to produce a clean signal.

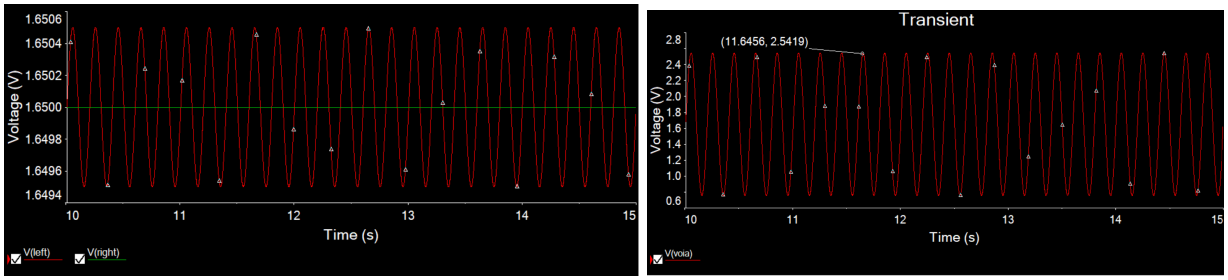

Fig. 15. Input Testing Signal to Instrumentation Amplifier and Integrator Section, Simulated VOIa from Instrumentation Amplifier

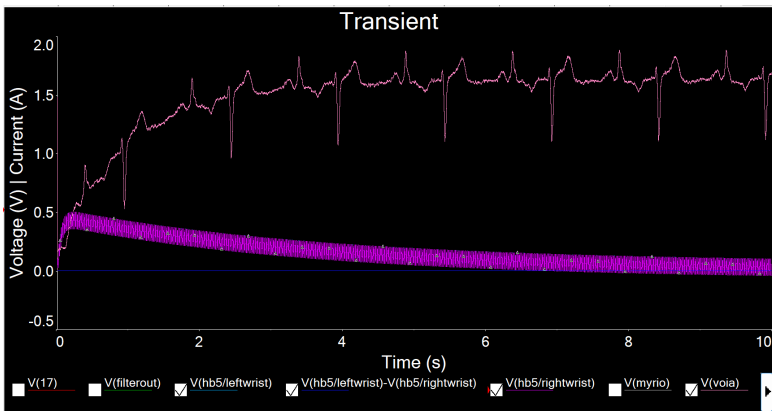

Fig. 16. Inamp Output with EKG Signal (pink)

IV. Layout

We took into consideration variables such as logical part arrangement, organization and thoroughness of power supply tracking, test point strategy, and bypass capacitor locations to choose the board layout shown in Fig. 17.

We decided to put the power supply components in the top right of the board because the battery took up a lot of space that would best be saved in the corner. Since only one side of the battery is connected, we save a lot of space as shown in Fig. 17 Either corner would have been fine, but we decided to put these components in the right corner because the isolation components had more connections to the top section of U17.

One of the most important decisions in designing a board is choosing where to put the amplifiers because they connect many components in the system. We chose to put the in-amp amplifiers, U1 and U2 near the jacks, the filter amp, U7, somewhere in the middle, and the isolation amps at the top. These placements allowed for short connections and a logical flow through the circuit. We also all made sure to place the bypass capacitors close to their corresponding op amps. This is important because it reduces the power supply noise and limits the effects of voltage spikes.

Another aspect to consider when designing a board is assembly and debugging simplicity. This is why we chose to design the board with all amplifiers accept U15 facing the same direction. This will minimize mistakes when the boards are assembled by 3W Electronics, and this will minimize mistakes when we insert the amplifiers and test the boards. Additionally, there is symmetry across the board and the components are separated into groups based on their function. A majority of the power traces are also on the same plane, the copper bottom, which will likely lead to less interference with the other, regular traces. The silkscreen labels on this board are all adjacent to the components and will not be covered up by them once they are in place. The capacitors connected to the input jacks were located close to the jacks and the components they connect to. This is important as the traces carry extremely small voltages and need to be short to minimize losses and interference.

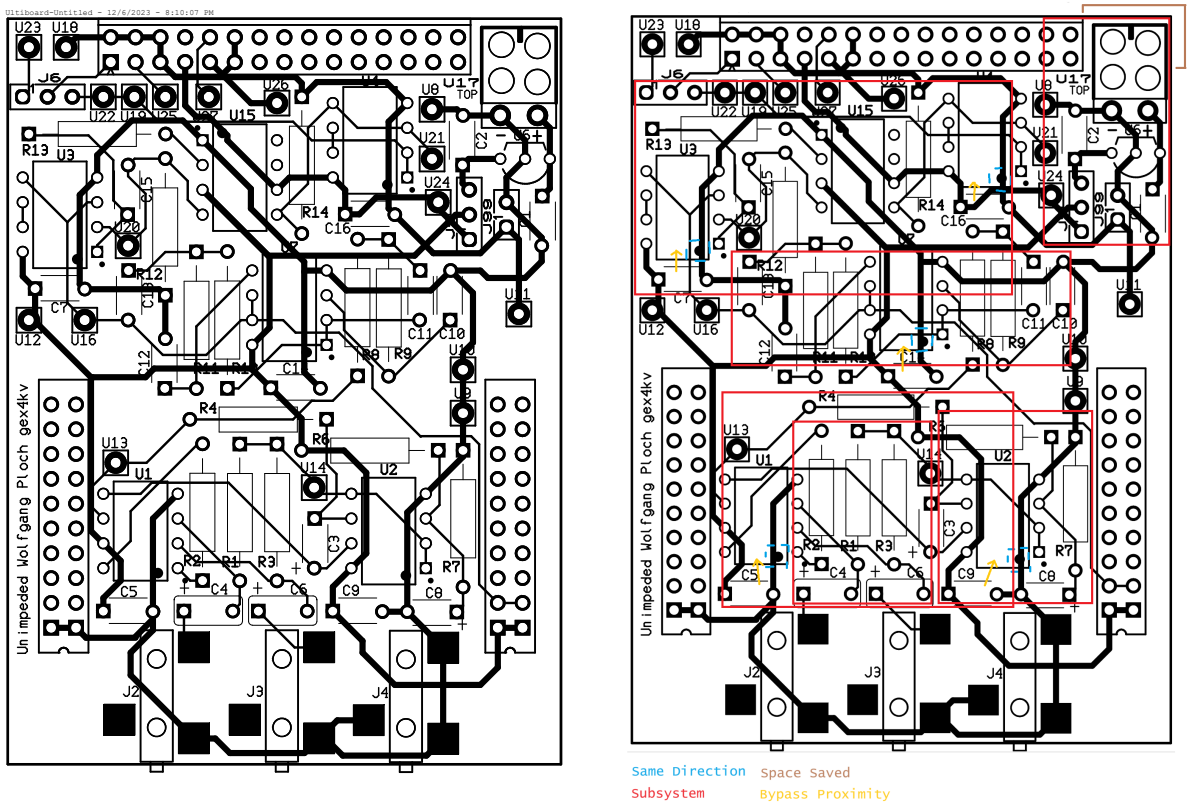

Fig. 17. Board Layout Silkscreen, Top/Bottom Copper Layers and Annotated

To validate the design of our board, we ran a connectivity check, which verifies whether all components have their necessary electrical connections, and a Design Rule Check (DRC)/Netlist check, which verifies whether the design falls within the the specific constraints for the board to be manufactured. These checks were done in Ultiboard. However, since the boards were designed and verified by the same party we wanted another party to also verify our boards.

To get a third-party verification. We decided to use FreeDFM. Free design software that verifies a PCB board is free of manufacturing issues. For FreeDFM to process out board, we first exported it to a Gerber file format. Gerber files contain the complete description of PCB layers and are the standard for communicating circuit board designs. After being verified by FreeDFM as shown in Fig. 18 and verified by Ultiboard, we were confident in the soundness of our design. However, these checks do not verify our calculations.

Fig. 18. FreeDFM Results

V. Assembly and Testing

In this section we explain our experience with assembling, troubleshooting, and testing the EKG System. The EKG system is shown in Fig. 24.

Some of the difficulties we ran into during testing was simply figuring out how to connect the different grounds and supplies while testing the different parts of the board. While we did figure it out while testing, it would have been helpful to familiarize ourselves with it sooner. Another issue we ran into was a mixed up reference designator. The resistor markers for one of the input RC filter resistors and the gain resistor got mixed up when designing the silkscreen, this was also transferred over to the assembly guide. Once this problem was discovered, the resistors were simply replaced by desoldering them and resoldering them. Another issue we ran into is the fact that the gain values of the isolator drifted so much from the predicted ones that our isolator didn't work. This was the biggest discrepency between our predicted and simulated circuit, where everything functioned as expected, and our physical board. The section on testing the isolator dives deeper into this issue.

A. Testing Setup and Experience

At the beginning of testing we only had the board assembly by WWW and the opamps. We do not have the battery at this point so we used the AD2 to provide power by shunting J5 3.3Vin and 3.3Vout and shunting the J99 pins.

1) Power Supply: We tested the power supply shown in Fig. 1 by connecting a 9V battery to 9Vin (or J0) and measuring the output at U12[5]. The expected measurements at the test points are outlined below.

- Test-Point: U12
- Calculated Values: 3.3 volts
- Simulated Values: 3.3 volts
- Predicted Freq Response: N/A
- Expected Tolerance on Values: +/- 0.1 volts

- Test-Point: U24
- Calculated Values: 3.3 volts
- Simulated Values: 3.3 volts
- Predicted Freq Response: N/A
- Expected Tolerance on Values: +/- 0.1 volts

2) Isolator: We tested the isolator by removing all ICs from the board except for U15, U3, and U4 as these three make up the isolator subsystem. The two grounds of the circuit were connected using J99 and a jumper to enable the AD2 to power both sides of the circuit. The positive power supply of the AD2 was set to 3.3 volts and connected to U24 and the ground of the AD2 was connected to U10. The wavegen of the AD2 was connected to the first channel input as well as U16, the second channel of the AD2 was connected to U19. A 5 Hz sine wave with an amplitude of 1.25 volts and a DC offset of 1.65 was created with the wavegen and the output of the isolator was measured. The expected measurements at the test points are outlined below.

The expected values from the calculations and Multisim values did not match the actual values that we were able to obtain from the actual circuit. The output ended up clipping around halfway through the sine wave and the output was unusable. We were unaware that the K gain values for the isolator chip are volatile and not guaranteed to be a certain value. We solved

this problem by building the isolator circuit on a breadboard and trying values until we ended up with a working circuit. The values that we settled on were $82k\Omega$ for R_{12}, $68k\Omega$ for R_{14}, and 56Ω for R_{13}. The reason that the value for R_{13} was lowered is because we overlooked a design tip, chose the resistor value so that it has a 0.5 volt drop across it when the LED has its maximum current flowing through it. Using the fact that the LED has a maximum current of 10 mA and Ohm's law, the value was calculated to be 50Ω. A 56Ω resistor was chosen for it.

- Test-Point: **U20**
- Calculated Values:
  - Sine wave with amplitude of 1.25 volts and an offset of 1.65 volts with a frequency of 100 Hz.
- Simulated Values:
  - Sine wave with amplitude of 1.25 volts and an offset of 1.65 volts with a frequency of 100 Hz.
- Predicted Freq Response:
  - No filter so theoretically no frequency response
- Expected Tolerance on Values: +/-0.1 volts

- Test-Point: **U22**
- Simulated Values: Shown in Fig 3
- Expected Tolerance on Values: +/-10%
- R14 was the DNI value. The voltage amplitude at the input of the isolator during testing will be used to calculate the value for R14 if it needs to be changed. A value of 18k was used during testing. If a new value needs to be calculated, the formula used to find 18k will be used: R2 = (R1*G)/K3

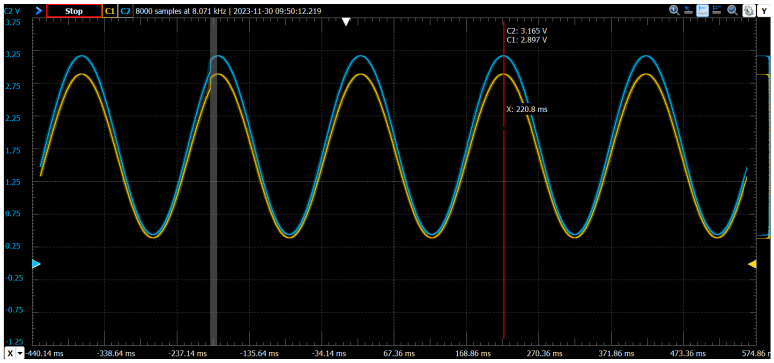

Fig. 19. Isolator Transient Showing the Input Signal (Orange) and the output signal (Blue) with the Peak Amplitudes Marked

3) Butterworth Filter: To test the butterworth filter system shown in Fig. 4. Inserted the dual op-amp U7, then connected the function generator to Vin. The first scope channel was connected to Vin. The second scope channel was connected to Vout. We then ran an AC Sweep to confirm the shape and Q value of the filter. The expected measurements at the test points are outlined below.

- Test-Points: Filter
- Input: U14 from the instrumentation amplifier.
- Output: U16
- Calculated Values:
  - Input: 1.65 VDC with varying sine wave of amplitude 1.25 volts. Break point of roughly 62.64 Hz.
- Simulated Values:
  - Input: 1.65 VDC with varying sine wave of amplitude 1 volts. Break point of roughly 59.8 Hz.
- Predicted Freq Response:
  - 4th order low pass filter with a break point of roughly 60 Hz.
- Expected Tolerance on Values:
  - The break point will most likely be +/- 3Hz from the expected value.
- Troubleshooting:
  - Check the dot on U7 and verify the op amp is facing south.

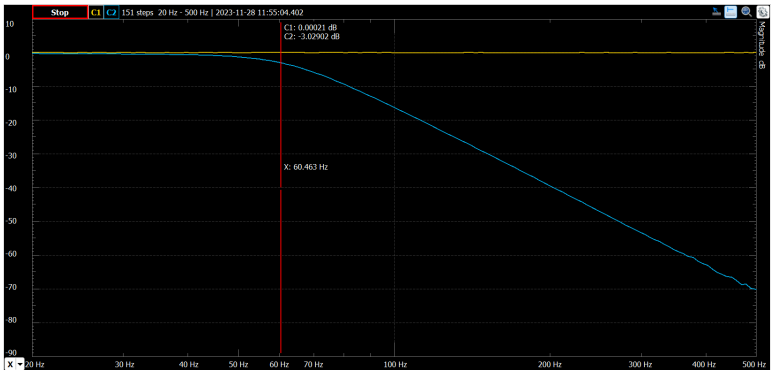

Fig. 20. Butterworth Filter AC Sweep from 20 Hz to 500 Hz with the break point frequency indicated

4) Integrator Offset (Vmid): This subsystem provides the offset to the instrumentation amplifier. To test the integrator offset as shown in Fig. 7, we first inserted U2, ensuring the dot is correctly aligned facing south of the board. We then connected the first AD2 channel to VCC33 and the second to Vmid (U14). We wanted to validate that the output of this subsystem is half VCC33 as calculated. The expected measurements at the test points are outlined below.

- Test-Point: **U14**
- Calculated Values: VCC33 / 2 = 1.65 volts DC
- Simulated Values: 1.651 volts DC
- Predicted Freq Response: The filter created by C8 is first order and has a breakpoint frequency of 3.18 Hz. This filter is low pass so the higher interference signals will get attenuated. This value will likely not fluctuate much. Low pass first order, breakpoint of 3.18 Hz.
- Expected Tolerance on Values: Based on 5% resistors: +/-0.825 volts
- Troubleshooting:
  - Validate U2 orientation.
  - Validate resistor and capacitor component values within 10%.
  - Validate there is no railing within the in amp.

Fig. 21. Vmid Measurements

5) RC Filters: To test the RC network filters shown in Fig. 6. All RC filter components should already be inserted. The input filters each create a first order high pass filter. We connected the wave generator and the first channel to the left side of J2 and the second channel to the junction of C4 and R2 to test the first RC system. We did the same for J3 and the junction of C6 and R3 for the second RC system. We then validated the input filters with an AC sweep to determine the corner frequency. The expected measurements at the test points are outlined below.

- Input:
  - Circuit 1: Left side of J2
  - Circuit 2: Left side of J3
- Output:
  - Junction of C4 and R2
  - Junction of C6 and R3
- Predicted Frequency Response: 1st order highpass filter with f_c = 0.059 Hz
- Simulated Frequency Response: f_c = 0.059 Hz with a 0dB passband.
- Troubleshooting:
  - Q: Corner frequency is off by more than 10%.
    - A: With a multimeter, check the resistance and capacitance values to ensure proper components.

6) Instrumentation Amplifier: To test the instrumentation amplifier all IC's were removed accept for U1 and U2. The output was measured at U13. We were having some issues with an increasing feedback so one thing we wish we did in the development process was add a test points at the input of the input of the i-amp where the RC junction is. This would allow us to better test the RC and i-amp systems separately. The expected measurements at the test points are outlined below. These measurements align with our simulations in Fig. 15. We ended up removing the gain resistor of the I-amp completely to make the gain of the amp unity. In hindsight, this was probably the best value to chosen for the "Do not install value". Our AD623 did not like the lack of gain resistor for some reason, we ended up having clipping in weird regions if the amplitude of the input signal exceeded 250 mV. We placed a $100k\Omega$ resistor in the holes for the gain resistor to make the AD623 have a gain of 2. With this gain, we were able to get better looking output signals that did not clip.

- Test-Point: **U13**
- Calculated Values:
  - 1.65 volts DC offset with a sine wave of amplitude 1 volt and frequency of 100 Hz superimposed on it.
- Simulated Values:
  - 1.65 volts DC offset with a sine wave of amplitude 1 volt and frequency of 100 Hz superimposed on it.
- Predicted Freq Response:
  - First order high pass filter with a break point of 0.059 Hz.
- Expected Tolerance on Values:
  - The sine wave will have an amplitude from 0.9 to 1.1 volts due to the tolerance of the gain resistor.

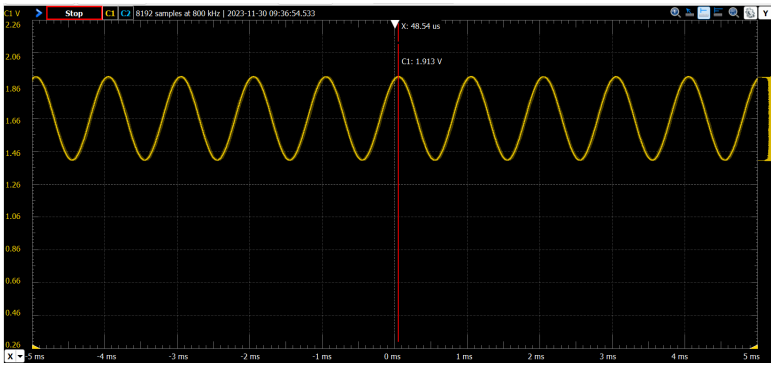

Fig. 22. Instrumentation Amplifier Test Showing the Output with Two 180 Degree Out of Phase 500 mV Sine Waves as Inputs

7) Integrator: To test the integrator as shown in Fig. 7, we connected the wave generator on U13 as well as channel 1 of the AD2. Before carrying out the run we verified the offset voltage at Vmid with U14. We then connected channel 2 of the AD2 to the output of U2B. The Integrator was tested with the Iamp in Fig. 15. The expected measurements at the test points are outlined in the Iamp Section.

B. EKG Testing

To test the EKG signal we put together the setup shown in Fig. 23. Electrode stickers were attached to the back of both wrists and one on the ankle. The wrist electrodes were connected to both input jack through the alligator clip to input jack cables. The ankle electrode was connected to the ground jack in the same manner. During testing we noticed that the test subject had to relax their arms and stay still. If the subject clenched their hands or held them at uneven levels, this would produce variability in the readings making the results inconsistent. Since the electrodes are sticky and not as accurate when reapplied, we were careful to apply the electrodes and collect data in one session. The electrodes were connected to the finalized board shown in Fig. 24. This board was soldered and assembled by 3W Electronics with some parts such as resistors and capacitors soldered by us.

C. Data Capture and Results

We took several ECG measurements of each of our heartbeats and a portion of one of these is shown in Fig. 25. We followed the setup shown in Fig. 23. The data was gathered at a horizontal rate of 500mS per division, yielding 8000 samples at 1.6KHZ samples per second. At first, the signal was very noisy and the pulse of the heart was only faintly visible as shown in Fig. 25. To produce a clearer signal, we designed a FIR moving average filter that eliminated the 60Hz interference. This yielded a

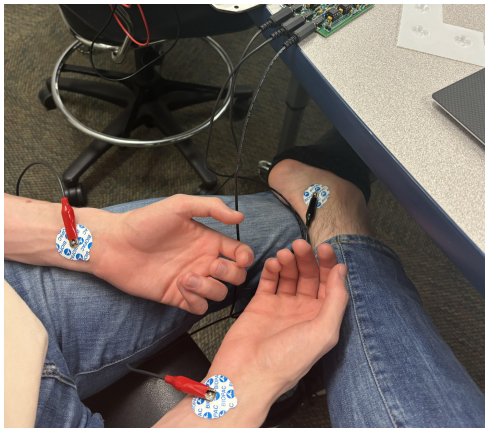

Fig. 23. EKG Test Setup

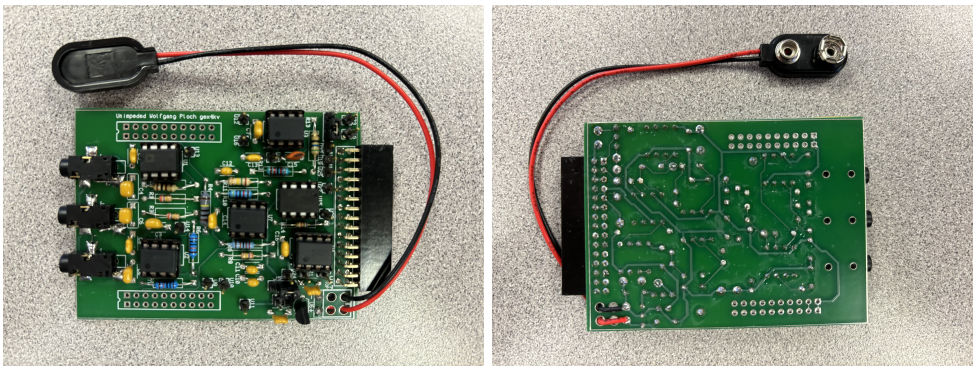

Fig. 24. Front and Back View of EKG System

much cleaner signal of the heart's pulses as shown in Fig. 26. We intentionally choose to filter out the noise at 60Hz knowing how, especially in a modern classroom, where the samples were taken, we are surrounded by 60Hz waves from sources such as the power outlets and lights.

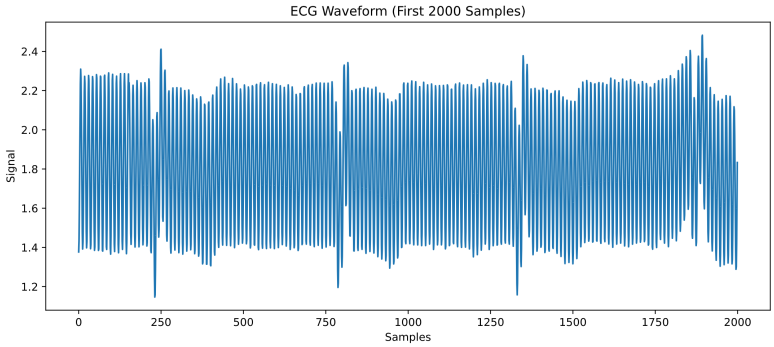

Fig. 25. Front and Back View of EKG System

When building the moving average filter for 60Hz, we first found its kernel size. We solved for N, using n=1 to find the number of elements in out kernel. The sampling frequency in this case is the nyquist rate fs/2 = 800Hz. Plugging this in, and setting our signal of interest to 60Hz, we find N to be 13.33. Because N is not an natural number, we decided to convolve two moving average filters using N = 13 and N = 14. Since n is the inverse of N this means that we will filter out noise at every 1/13 and 1/14th interval of pi. Convolving these two filters will remove signals closer to exactly 60Hz. This process of recording and filtering data was repeated for all group members, and, as mentioned prior, an example of these results is shown in Fig. 26. It was necessary to have a moving average filter at both size 13 and 14, because as shown in the frequency response plot Fig. 27, the convolution of both these filters creates a null that properly attenuates 60Hz. The code for the FIR filter is shown in Fig. 29.

$$\frac{2\pi f}{f_s} = \frac{2\pi n}{N} \Rightarrow \frac{2\pi * 60}{1.6kHz/2} = \frac{2\pi * 1}{N} \Rightarrow N = 13.333$$

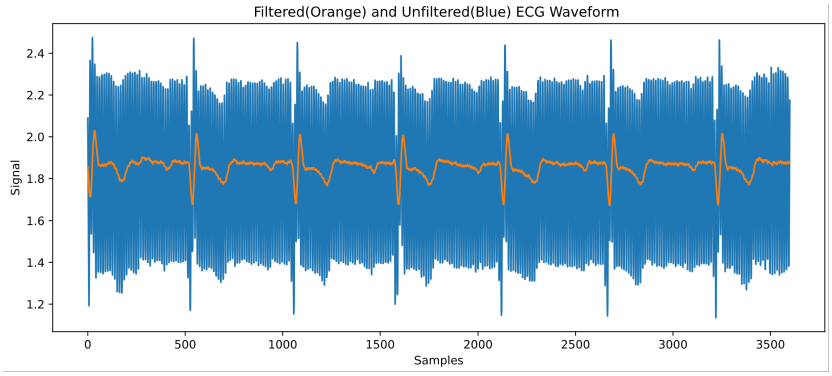

Fig. 26. Filtered ECG Signal

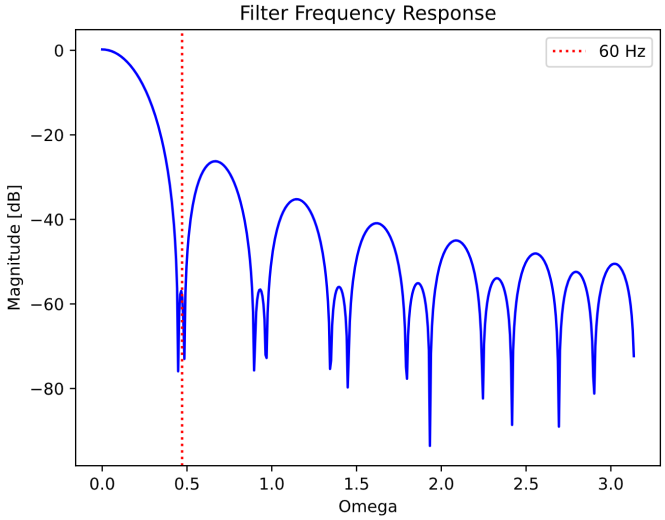

Fig. 27. ECG Signal Frequency Response

VI. Conclusion

Overall we were effectively able to design a multi-component system to create an EKG signal. We took into consideration, power and current limitations, and gain and power requirements using the datasheets. We ran into some physical issues with the isolator, but were able to experimentally solve it.

We thought this was a very cool project drawing on many topics we covered we covered throughout the semester. We utilized our understanding of fundamental circuit laws, digital signal processing, industry standard circuits like inamps, and filter design. We also developed our skills to design multi-component systems with constraints, utilize the datasheets of unknown components like the isolator, design circuit boards with proper methods, and troubleshoot large systems. Throughout the project we gained important conceptual skills and hands-on industry experience like writing an assembly plan for 3W Electronics, using FreeDFM, and following a conservative and well-planned test plan.

In the future, we would love to see more freedom in choosing components, because this would provide varied constraints for students and students would have to research into those constraints to find out what the best tradeoff is. There could even be a tradeoff plan between multiple dual-op amp, voltage regulator, resistor etc.. components and why someone should use one over the other. We would also like to see less constraints on board layout as we believe maneuvering some of the initially locked items like the MSP430 (U98 and U99) would open up a lot of space for more creative designs while still being on the same footprint.

Our advice to future students for this project is to think ahead. We were not thinking about testing as we were designing the board so when we had to troubleshoot the board, we didn't have testpoints in the right place, like the input to the inamp. Taking the time to add the right testpoints, to choose the right components to leave out during assembly, and to double check calculations will make the debugging process a lot smoother. Overall, our design flow was pretty smooth as we were designing each stage of the board. Once we got the circuit board, debugging and finding areas we may have overlooked took was more intensive leading to the project feeling back-loaded. Putting more thought into how the physical circuit would behave and looking where multisim or our predicted values may overlook something, such as with the isolator, would have made the workflow a little easier.

Overall we enjoyed the project and felt it reinforced the concepts we learned throughout the year. We were able to make a successful and functional project.

VII. References

References

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VIII. Appendix

```
import numpy as np

fc_target = 63
Q_target = 0.5412
f_tolerance = 5
Q_tolerance = 0.06

R_vals =  [47000, 56000, 68000, 82000, 100000, 120000, 150000, 180000, 220000,
           270000, 330000, 390000, 470000, 560000, 680000, 820000, 1000000]
C_vals =  [10**(-6), 10**(-7), 10**(-8)]

for r1 in R_vals:
    for c1 in C_vals:
        for c2 in C_vals:
            for r2 in R_vals:

                m = r1/r2
                n = c2/c1
                Q = ((n*m)**0.5)/(m+1)
                fc = 1/(2*(np.pi)*c1*r2*((m*n)**0.5))

                fc_diff = abs(fc_target - fc)
                Q_diff = abs(Q_target - Q)

                if ((fc_diff <= f_tolerance) and (Q_diff <= Q_tolerance)):
                    print("Start of Possibility")
                    print("m value: "+str(m))
                    print("n value: "+str(n))
                    print("fc value: "+str(fc))
                    print("Q value: "+str(Q))
                    print("R1 value: "+str(r1))
                    print("R2 value: "+str(r2))
                    print("C1 value: "+str(c1))
                    print("C2 value: "+str(c2))
                    print("End of Possibility")
```

Fig. 28. Code Lisitng of the Python Program Written to Calculate the Resistor and Capacitor Values for the Butterworth Filters

```
'''
# nyquist = 1.6K /2 = 800 samples/second
# omega= 2pi*60/800
# 2pi*60/800 = 2pi*n / N, starting n at 1, 6/80 = 1/N, N = 80/6 = 13.33 -> N={13,14}
'''
# Load the CSV file
loaded_csv = np.genfromtxt('EKG_Data_2.csv', delimiter=',')

freq = 1600     # Hz
fs = freq / 2   # Nyquist Rate
f_null = 60     # Hz

N = 1 / (f_null / fs)

# Calculate Kernels
N1 = math.floor(N)
n1 = (60)/800
n1_array = [n1] * N1

N2 = math.ceil(N)
n2 = (60)/800
n2_array = [n2] * N2

# Convolve
filter = np.convolve(n1_array, n2_array)
filtered_ecg = np.convolve(filter, ecg_signal)

w, h = sp.signal.freqz(filter)
i=0
while i < len(w):
  w[i] = w[i]
  i+=1

# Plot Filtered Signal
plt.figure().set_figwidth(plt_fig_width)
plt.plot(ecg_signal[2400:6000]) # only plot second 2000 samples
plt.plot(filtered_ecg[2400:6000])
plt.title('Filtered(Orange) and Unfiltered(Blue) ECG Waveform ')
plt.xlabel('Samples')
plt.ylabel('Signal')
plt.show()
```

Fig. 29. FIR Filter Code